REMARKS

In response to the Examiner's Action mailed October 4, 2002, Applicants amend their application and request reconsideration. In this Amendment no claims are cancelled so that claims 10, 11, and 17-14 are pending. A complete clean copy of the pending claims appears in the appendix.

Included with the Official Action were two PTO-1449 forms pertaining to two Information Disclosure Statements filed at different times. The Information Disclosure Statement filed September 5, 2002 cited a single U.S. Patent that was mentioned in a search report of a corresponding application in another country. The PTO-1449 form accompanying that Information Disclosure Statement was returned but without the Examiner's initials indicating the consideration of that reference. Applicants respectfully request that another copy of the PTO-1449 including initials indicating consideration of the single cited reference be supplied in the next communication.

Claims 10 and 11 were rejected as not supported by the application as filed, i.e., pursuant to 35 USC 112, first paragraph, and as indefinite pursuant to 35 USC 112, second paragraph. Both rejections are respectfully traversed.

In considering the rejection pursuant to the first paragraph of 35USC 112, it is difficult to understand the Examiner's position. The Examiner correctly noted that claims 10 and 11 are particularly supported by the disclosure of the patent application at pages 15-17. After extended study of the Examiner's comments and the specification, it was concluded that the word "continuously" may be the source of the Examiner's concern. Therefore, that word has been eliminated from both of claims 10 and 11. Further, claim 10 has been amended for clarity and explains that the element formerly referred to as a "protrusion" is really an internal lead. Thus, that claim has been amended for clarity as to that element.

With regard to the rejection pursuant to the first paragraph of 35 USC 112, the Examiner is directed to Figures 22-25 of the patent application that are described at pages 15-17 of the patent application. Figure 23 particularly shows the die pad on which the semiconductor chip 1 is mounted. The die pad in that depicted embodiment is rectangular and its entire extent can be determined from Figure 23. It is apparent that the leads 2 of the lead frame are only partially depicted in that Figure 23. However, it is plainly apparent from that figure, just as it is from Figure 25 in which the die pad extent is clearly apparent, that there is no connection between the die pad and the lead frame which incorporates the leads 2. The specification, as originally filed, includes the text of the application as well as the figures of the application. Thus, contrary to the Examiner's assertion, the specification does, in fact, disclose that the die pad is separate from and not connected to, continuously or otherwise, the lead frame as recited in claims 10 and 11.

The rejection pursuant to 35 USC 112, first paragraph is plainly erroneous and cannot be properly maintained.

The rejection of claims 10 and 11 pursuant to 35 USC 112, second paragraph, seems to be a restatement of the rejection just discussed. According to the Examiner, the cited language of the claims is confused and not understood. Again, the Examiner is referred to the description at pages 15-17 of the patent application and Figures 23 and 25 to which that description pertains.

It may be possible that the Examiner is not distinguishing the word "contact" from the word "connected". If so, the Examiner's attention is invited to any standard dictionary of the English language. Those two words have a clearly different meaning and they are properly used in claims 10 and 11. The word "connect" means "to join or fasten together; link; unite". The word "contact" means "the coming together or touching of two objects or surfaces". The differences are readily apparent. Two elements that are connected together are actually united or joined and cannot be taken apart without cutting or destruction of the elements. Elements that are in contact with each other are merely touching and can be separated from each other without destroying any bond or junction or destroying the elements themselves. It is apparent from Figures 22-25 of the patent application that the lead frame including the leads 2 is not connected to the die pads 3 that are illustrated in those figures (although not given reference numbers in Figure 23 and 25). It is just as apparent by the presence of the lines indicating the absence of a bond or junction, that the elements 2h and 2i are in contact with but not connected to the respective die pads 3. This arrangement is accurately and fully described in the original specification at pages 15-17 as well as in the figures. Therefore, the second rejection as to form with regard to claims 10 and 11 cannot be properly maintained and should be withdrawn.

The rejection of claim 21 as indefinite is overcome by amendment. Again, it appears that in examining the claim the Examiner did not distinguish between the tape member being "fixed" to the surface of the chip and the surface contacting the chip. The word "fixed" carries the same meaning as "connected". To avoid improper interpretation of the claim language, claim 21 has been amended, and claim 22 has been amended in the same way, to refer to the tape member as being in contact with the surface of the chip but not adhered to the surface of the chip. This language is clear and means that there is no adhesive material bonding the tape member to the chip surface. There is merely a touching between the tape member and the chip surface. This claim language is fully supported in the original disclosure at page 9, lines 15-18 where it is expressly stated that the tape member is bonded only to the internal lead and is not bonded to the semiconductor chip.

Claims 10 and 11, both independent claims, and claims 17 and 19, claims depending from claim 10, were rejected as anticipated by Tomita et al. (U.S. Patent 5,535,509, hereinafter Tomita). This rejection is respectfully traversed.

Turning first to claim 10, that claim cannot be anticipated by Tomita because Tomita does not describe all of the elements of that claim. Tomita, like the invention, is directed to a Lead on Chip (LOC) semiconductor chip mounting arrangement. Tomita does not, however, describe any lead frame including any internal leads that extend perpendicular to and contact the die pad. The Examiner directed attention to Figures 1A, 1B, 2, 3A-3C, 8, 9A, 9B, 11, 12A, 12B of Tomita in rejecting claims 10, 17, and 19 as anticipated. A diligent review of those figures and of the other figures of Tomita does not reveal any structure including a lead frame having a lead that is substantially perpendicular to and contacts the die pad. Thus, the rejection of those claims cannot be maintained.

Claim 18, the other dependent claim depending from claim 10, was rejected as unpatentable over Tomita in view of Aoki (U.S. Patent 5,834,691). This rejection is respectfully traversed.

It is apparent from the discussion at page 7 of the Official Action that the rejection of claim 18 is founded on the assumption that Tomita anticipates claim 10. Since there is no possibility that Tomita anticipates claim 10, the rejection of claim 18 cannot be properly maintained.

In rejecting claim 10, the Examiner directed attention to Figures 10A-10D of Tomita. Those figures cannot be considered without referring to Figure 11 to which they pertain. Figure 11 shows a frame for leads 81 connected to a frame for a die pad 82. The frame for a die pad 82 includes a die pad 1 on which a semiconductor chip 2 is mounted. The frame for leads 81 includes internal leads 3 that extend across part of the surface of the semiconductor chip 2. The frames 81 and 82 are connected together, in the embodiment of Figure 11, by a spot weld 17. Tomita describes numerous means by which the two lead frames can be connected together. For example, an adhesive illustrated in Figure 8 may be used to connect the two frames. A rivet 15, illustrated before riveting in Figure 9A of Tomita, may be used to make the connection as shown in Figure 9B of Tomita, after riveting. Yet a different technique for connecting the two lead frames is illustrated in Figures 10A-10D of Tomita. There, a tab 16 of the frame 82 is inserted through a slot 14 in the frame 81 and subsequently bent parallel to the frames, as shown in Figure 10D of Tomita, connecting the frames 81 and 82 together.

As already noted, anticipation requires that a reference describe every element of a claim. Claim 11 specifies, as already described in detail, that the die pad is *not* connected to the lead frame. The die pad of the frame 82 of Tomita is connected to the frame 81 including the leads by the technique illustrated in Figures 10A-10D of Tomita. Thus, Tomita cannot meet that limitation of claim 11 so that the rejection for anticipation is erroneous.

In addition, Tomita fails to describe the limitation of claim 11 specifying that the die pad include fixed protrusions extending toward and contacting some of the internal leads. Even

employing the attaching arrangement of Tomita's Figures 10A-10D, in place of the spot well 17 in Figure 11 of Tomita, it is apparent that no part of the die pad 1 protrudes from, much less contacts, any part of any internal lead 3. The Examiner is invited to compare not only Figures 10A-10D and 11 of Tomita to the final limitation of claim 11, but all figures of Tomita. Every die pad in every embodiment of Tomita is free of any kind of protrusion that might extend in a direction to come into contact with any internal lead 3. There can be no anticipation.

Therefore, on two independent grounds, Tomita cannot anticipate claim 11.

Claim 22 was rejected as anticipated by Ichinose (U.S. Patent 6,211,573). This rejection is respectfully traversed.

Figure 22 seems to be the most pertinent figure of Ichinose to claim 22. However, as described in Ichinose at column 40 lines 38-49, the tape members 3B are adhered to the surface of the semiconductor chip 4. Therefore, Ichinose cannot anticipate claim 22 as now pending.

Claims 20, 21, 23, and 24 were rejected as unpatentable over Ichinose in view of Lee this rejection is respectfully traversed.

In this group of claims, only claim 21 is an independent claim. That claim, like amended claim 22, describes that each of the tape members is in contact with the surface of the semiconductor chip but is not adhered to the semiconductor chip. As discussed above, that arrangement is not described by Ichinose and therefore Ichinose cannot anticipate claim 22. Claim 24 depends from claim 22. Claim 24 adds to claim 22 a limitation that only a portion of each tape member protrudes beyond a respective edge of the surface of the semiconductor chip. It is for that limitation, with respect to all four of the rejected claims, that Lee was cited. Although Applicants agree that the structure described in Lee includes tape members partially extending beyond the edge of the surface of the semiconductor chip, Lee does not supply the element of rejected claims 20-24 allegedly supplied by, but missing from, Ichinose.

The semiconductor device shown, for example, in Figure 5 of Lee includes an insulating layer 53 that poorly adheres to the semiconductor chip. The film is made of a fluorine containing polymer and is quite slippery. To improve adhesive forces, the surface of the insulating layer 53 is roughened, referred to as having an unevenness or as a knurled surface in Lee. This surface modification is said to improve the adhesive forces between the insulating layer 53 and the inner lead and between the insulating layer 53 and the semiconductor chip 51. (See column 5 lines 46-53 of Lee). It follows that Lee makes clear that the insulating layer 53 is adhered to the semiconductor chip 51 because the entire object of Lee is to improve the adhesion between these two elements. Thus, Lee cannot supply the limitation of each of claims 20-24 regarding the contact without adhesion of the tape members and the surface of the semiconductor chip. Stated another way, the combination of Ichinose and Lee cannot include all

of the limitations of any of claims 20-24 and therefore cannot establish *prima facie* obviousness of any of those claims.

Moreover, by omitting any adhesive material used in the prior art, between the tape element and the semiconductor chip, numerous advantages are realized in the invention. Ionic impurities contained within an adhesive can reduce the resistance of the semiconductor device to moisture absorption. The absence of an adhesive prevents that moisture absorption problem that would be experienced by Ichinose and Lee. The absence of any bonded connection between the semiconductor chip and the tape member eliminates the cost of the bonding material and its application as well as reducing strain or distortion in response to stresses applied by the bonded wires. These advantages which cannot be found in or even derived from any combination of Ichinose and Lee, further demonstrating that claims 20-24 are patentable over those references.

Reconsideration and withdrawal of the rejection as well as allowance of the remaining claims, claims 10, 11, and 17-24, are appropriate and earnestly solicited.

Respectfully submitted,

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